



PSoC® Creator™

Project Datasheet for

PredlogaInstrument_42KIT049_001

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1 Overview

The Cypress PSoC 4 is a family of 32-bit devices with the following characteristics:

- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals such as PWM, UART, SPI and I2C
- Analog subsystem that includes 12-bit SAR ADC, comparators, op amps, CapSense, LCD drive and more
- Several types of memory elements, including SRAM and flash
- Programming and debug system through Serial Wire Debug (SWD)
- High-performance 32-bit ARM Cortex-M0 core with a nested vectored interrupt controller (NVIC)
- Flexible routing to all pins

Figure 1 shows the major components of a typical [PSoC 4200](#) series member PSoC 4 device. For details on all the systems listed above, please refer to the [PSoC 4 Technical Reference Manual](#).

Figure 1. PSoC 4200 Device Series Block Diagram

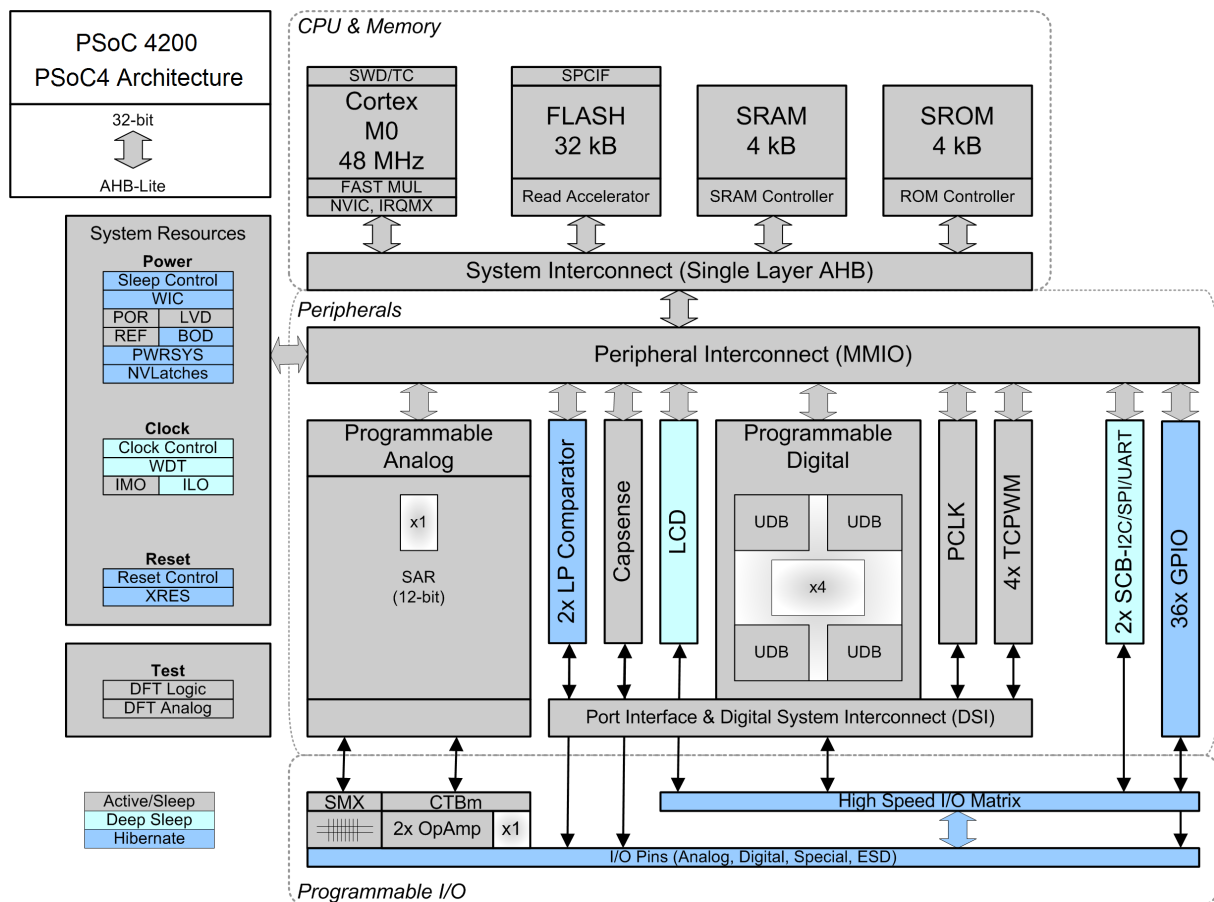


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C4245AXI-483
Package Name	44-TQFP
Family	PSoC 4
Series	PSoC 4200
Max CPU speed (MHz)	48
Flash size (kB)	32
SRAM size (kB)	4
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celsius)	-40 to 85

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by HFCLK, listed in the [System Clocks](#) section below.

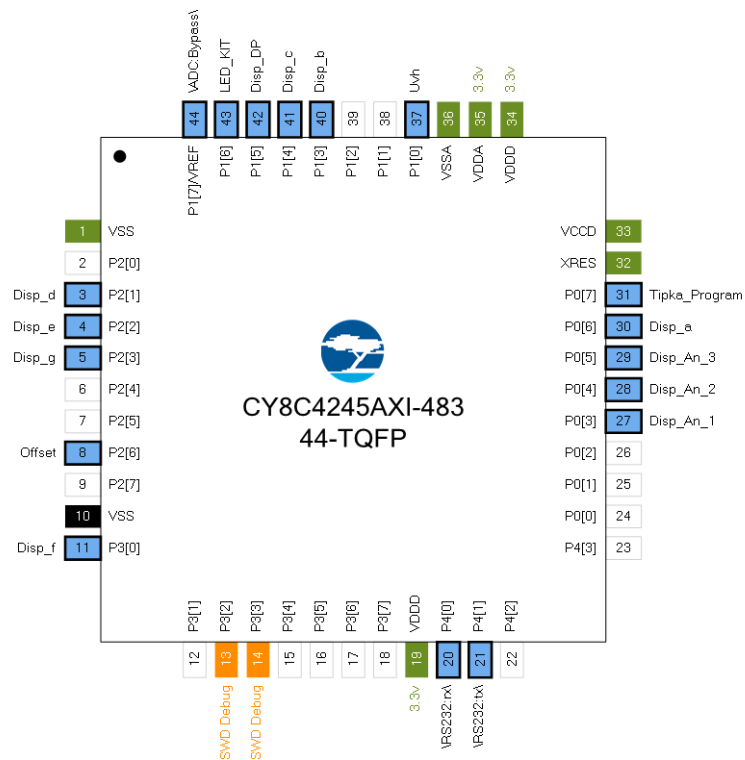
Table 2 lists the device resources that this design uses:

Table 2. Device Resources

Resource Type	Used	Free	Max	% Used
Digital Clocks	1	3	4	25.00 %
Interrupts	1	31	32	3.13 %
IO	20	16	36	55.56 %
Segment LCD	0	1	1	0.00 %
CapSense	0	1	1	0.00 %
Die Temp	0	1	1	0.00 %
Serial Communication (SCB)	1	1	2	50.00 %
Timer/Counter/PWM	0	4	4	0.00 %
UDB				
Macrocells	6	26	32	18.75 %
Unique P-terms	6	58	64	9.38 %
Total P-terms	6			
Datapath Cells	2	2	4	50.00 %
Status Cells	1	3	4	25.00 %
StatusI Registers	1			
Control Cells	1	3	4	25.00 %
Control Registers	1			
Comparator/Opamp	1	1	2	50.00 %
LP Comparator	0	2	2	0.00 %
SAR ADC	1	0	1	100.00 %
DAC				
7-bit IDAC	0	1	1	0.00 %
8-bit IDAC	0	1	1	0.00 %

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode
1	VSS	VSS	Power	
2	P2[0]	GPIO [unused]		
3	P2[1]	Disp_d	Software In/Out	Strong drive
4	P2[2]	Disp_e	Software In/Out	Strong drive
5	P2[3]	Disp_g	Software In/Out	Strong drive
6	P2[4]	GPIO [unused]		
7	P2[5]	GPIO [unused]		
8	P2[6]	Offset	A/D Out	HiZ analog
9	P2[7]	GPIO [unused]		
11	P3[0]	Disp_f	Software In/Out	Strong drive
12	P3[1]	GPIO [unused]		
13	P3[2]	Debug:SWD_IO	Reserved	
14	P3[3]	Debug:SWD_CK	Reserved	
15	P3[4]	GPIO [unused]		
16	P3[5]	GPIO [unused]		
17	P3[6]	GPIO [unused]		
18	P3[7]	GPIO [unused]		
19	VDDD	VDDD	Power	
20	P4[0]	\RS232:rx\	Dgtl In	HiZ digital
21	P4[1]	\RS232:tx\	Dgtl Out	Strong drive
22	P4[2]	GPIO [unused]		
23	P4[3]	GPIO [unused]		
24	P0[0]	GPIO [unused]		
25	P0[1]	GPIO [unused]		
26	P0[2]	GPIO [unused]		
27	P0[3]	Disp_An_1	Software In/Out	Strong drive
28	P0[4]	Disp_An_2	Software In/Out	Strong drive
29	P0[5]	Disp_An_3	Software In/Out	Strong drive
30	P0[6]	Disp_a	Software In/Out	Strong drive
31	P0[7]	Tipka_Program	Software In/Out	Res pull up
32	XRES	XRES	Dedicated	
33	VCCD	VCCD	Power	
34	VDDD	VDDD	Power	
35	VDDA	VDDA	Power	
36	VSSA	VSSA	Power	
37	P1[0]	Uvh	Analog	HiZ analog
38	P1[1]	GPIO [unused]		

Pin	Port	Name	Type	Drive Mode
39	P1[2]	GPIO [unused]		
40	P1[3]	Disp_b	Software In/Out	Strong drive
41	P1[4]	Disp_c	Software In/Out	Strong drive
42	P1[5]	Disp_DP	Software In/Out	Strong drive
43	P1[6]	LED_KIT	Dgtl Out	Strong drive
44	P1[7]/VREF	\ADC:Bypass\	Analog	HiZ analog

Abbreviations used in Table 3 have the following meanings:

- A/D Out = Analog / Digital Output
- HiZ analog = High impedance analog
- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- Dgtl Out = Digital Output
- Res pull up = Resistive pull up

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode
P0[0]	24	GPIO [unused]		
P0[1]	25	GPIO [unused]		
P0[2]	26	GPIO [unused]		
P0[3]	27	Disp_An_1	Software In/Out	Strong drive
P0[4]	28	Disp_An_2	Software In/Out	Strong drive
P0[5]	29	Disp_An_3	Software In/Out	Strong drive
P0[6]	30	Disp_a	Software In/Out	Strong drive
P0[7]	31	Tipka_Program	Software In/Out	Res pull up
P1[0]	37	Uvh	Analog	HiZ analog
P1[1]	38	GPIO [unused]		
P1[2]	39	GPIO [unused]		
P1[3]	40	Disp_b	Software In/Out	Strong drive
P1[4]	41	Disp_c	Software In/Out	Strong drive
P1[5]	42	Disp_DP	Software In/Out	Strong drive
P1[6]	43	LED_KIT	Dgtl Out	Strong drive
P1[7]/VREF	44	\ADC:Bypass\	Analog	HiZ analog
P2[0]	2	GPIO [unused]		
P2[1]	3	Disp_d	Software In/Out	Strong drive
P2[2]	4	Disp_e	Software In/Out	Strong drive
P2[3]	5	Disp_g	Software In/Out	Strong drive
P2[4]	6	GPIO [unused]		
P2[5]	7	GPIO [unused]		
P2[6]	8	Offset	A/D Out	HiZ analog
P2[7]	9	GPIO [unused]		
P3[0]	11	Disp_f	Software In/Out	Strong drive
P3[1]	12	GPIO [unused]		
P3[2]	13	Debug:SWD_IO	Reserved	
P3[3]	14	Debug:SWD_CK	Reserved	
P3[4]	15	GPIO [unused]		
P3[5]	16	GPIO [unused]		
P3[6]	17	GPIO [unused]		
P3[7]	18	GPIO [unused]		
P4[0]	20	\RS232:rx\	Dgtl In	HiZ digital
P4[1]	21	\RS232:tx\	Dgtl Out	Strong drive
P4[2]	22	GPIO [unused]		

Port	Pin	Name	Type	Drive Mode
P4[3]	23	GPIO [unused]		

Abbreviations used in Table 4 have the following meanings:

- Res pull up = Resistive pull up
- HiZ analog = High impedance analog
- Dgtl Out = Digital Output
- A/D Out = Analog / Digital Output
- Dgtl In = Digital Input
- HiZ digital = High impedance digital

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type
\ADC:Bypass\	P1[7]/VREF	Analog
\RS232:rx\	P4[0]	Dgtl In
\RS232:tx\	P4[1]	Dgtl Out
Debug:SWD_CK	P3[3]	Reserved
Debug:SWD_IO	P3[2]	Reserved
Disp_a	P0[6]	Software In/Out
Disp_An_1	P0[3]	Software In/Out
Disp_An_2	P0[4]	Software In/Out
Disp_An_3	P0[5]	Software In/Out
Disp_b	P1[3]	Software In/Out
Disp_c	P1[4]	Software In/Out
Disp_d	P2[1]	Software In/Out
Disp_DP	P1[5]	Software In/Out
Disp_e	P2[2]	Software In/Out
Disp_f	P3[0]	Software In/Out
Disp_g	P2[3]	Software In/Out
GPIO [unused]	P0[1]	
GPIO [unused]	P0[0]	
GPIO [unused]	P1[1]	
GPIO [unused]	P1[2]	
GPIO [unused]	P0[2]	
GPIO [unused]	P2[0]	
GPIO [unused]	P3[1]	
GPIO [unused]	P3[4]	
GPIO [unused]	P2[7]	
GPIO [unused]	P2[5]	
GPIO [unused]	P2[4]	
GPIO [unused]	P3[7]	
GPIO [unused]	P4[2]	
GPIO [unused]	P4[3]	
GPIO [unused]	P3[5]	
GPIO [unused]	P3[6]	
LED_KIT	P1[6]	Dgtl Out
Offset	P2[6]	A/D Out
Tipka_Program	P0[7]	Software In/Out

Name	Port	Type
Uvh	P1[0]	Analog

Abbreviations used in Table 5 have the following meanings:

- Dgtl In = Digital Input
- Dgtl Out = Digital Output
- A/D Out = Analog / Digital Output

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the [System Reference Guide](#)
 - CyPins API routines
- Programming Application Interface section in the [cy_pins component datasheet](#)

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Unused Bonded IO	Disallowed
Heap Size (bytes)	0x80
Stack Size (bytes)	0x0400
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD (serial wire debug)
Chip Protection	Open

3.3 System Operating Conditions

Table 8. System Operating Conditions

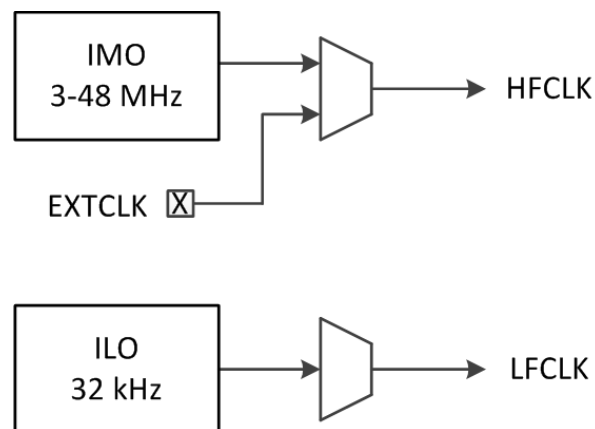
Name	Value
VDDA (V)	3.3
VDDD (V)	3.3
Variable VDDA	True

4 Clocks

The clock system includes these clock resources:

- Two internal clock sources:
 - 3 to 48 MHz Internal Main Oscillator (IMO) $\pm 2\%$ at 3 MHz
 - 32 kHz Internal Low Speed Oscillator (ILO) output
- HFCLK can be generated using an external signal from EXTCLK pin
- Twelve clock dividers, each with 16-bit divide capability:
 - Eight can be used for fixed-function blocks
 - Four can be used for the UDBs

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
DPLL_Sel	NONE	IMO	48 MHz	48 MHz	±2	True	True
SysClk	NONE	HFCIk	? MHz	48 MHz	±2	True	True
Direct_Sel	NONE	IMO	48 MHz	48 MHz	±2	True	True
PLL1_Sel	NONE	IMO	48 MHz	48 MHz	±2	True	True
PLL0_Sel	NONE	IMO	48 MHz	48 MHz	±2	True	True
HFCIk	NONE	Direct_Sel	48 MHz	48 MHz	±2	True	True
IMO	NONE		48 MHz	48 MHz	±2	True	True
LFCIk	NONE	ILO	? MHz	32 kHz	±60	True	True
ILO	NONE		32 kHz	32 kHz	±60	True	True
Timer2 (WDT2)	NONE	LFCIk	? MHz	? MHz	±0	False	False
ExtClk	NONE		24 MHz	? MHz	±0	False	False
DigSig3	NONE		? MHz	? MHz	±0	False	False
DigSig2	NONE		? MHz	? MHz	±0	False	False
DigSig4	NONE		? MHz	? MHz	±0	False	False
DigSig1	NONE		? MHz	? MHz	±0	False	False
Timer1 (WDT1)	NONE	LFCIk	? MHz	? MHz	±0	False	False
Timer0 (WDT0)	NONE	LFCIk	? MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

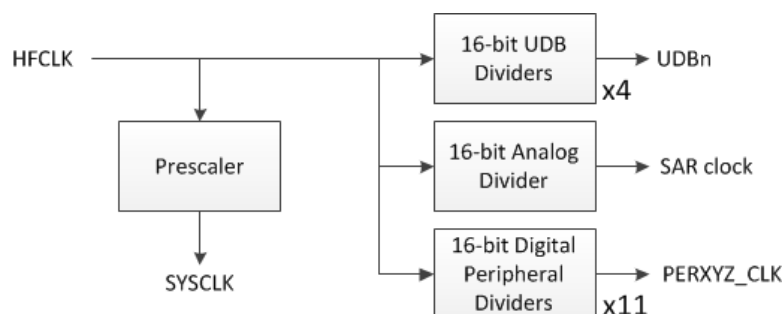


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
ADC_intClock	FIXED - FUNCTION	HFCIk	3 MHz	3 MHz	±2	True	True

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
RS232_SCBCLK	FIXED_ - FUNCTION	HFCIk	921.6 kHz	923.077 kHz	±2	True	True
Clock	DIGITAL	HFCIk	1 kHz	1 kHz	±2	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the [PSoC 4 Technical Reference Manual](#)
- Clocking chapter in the [System Reference Guide](#)
 - CySysClkImo API routines
 - CySysClkIlo API routines
 - CySysClkWrite API routines

5 Interrupts

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Intr Num	Vector	Priority
ADC_IRQ	14	14	3

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the [PSoC 4 Technical Reference Manual](#)
- Interrupts chapter in the [System Reference Guide](#)
 - CyInt API routines and related registers
- Datasheet for [cy_isr component](#)

6 Flash Memory

PSoC 4 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 12 lists the Flash protection settings for your design.

Table 12. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0xFFFF	W - Full Protection
0x1000	0x7FFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 128 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- W - Full Protection

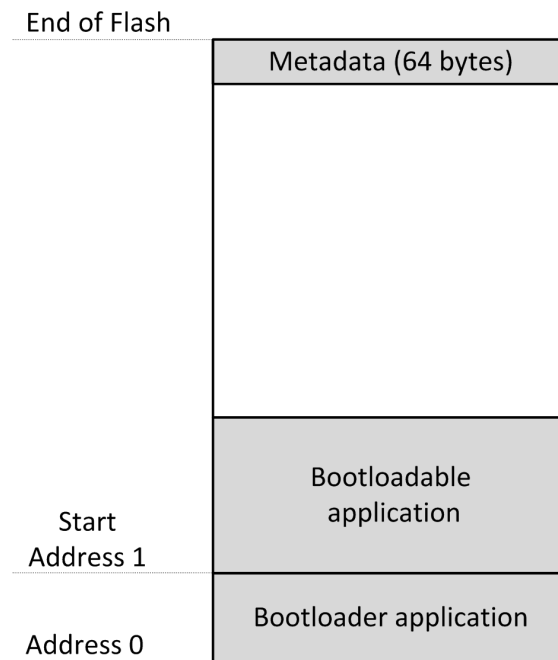
For more information on Flash memory and protection, please refer to:

- Flash Protection chapter in the [PSoC 4 Technical Reference Manual](#)
- Flash and EEPROM chapter in the [System Reference Guide](#)
 - CySysFlash API routines

7 Bootloader and Bootloadable

Figure 5 details the Flash memory map for the bootloader and/or bootloadable application(s) included in this design.

Figure 5. Bootloader Memory Map



7.1 Bootloadable Application

Table 13. Bootloadable Settings

Name	Value
Application Version	0x0001
Application ID	0x0000
Application Custom ID	0x0
Application Image 1 Start Address	0x1100
Application Image 1 End Address	0x7FFF
Manual Application Image Placement	False

7.2 Bootloader Application

Table 14. Bootloader Settings

Name	Value
Checksum Type	BasicChecksum
Supports Multiple Application Images	False
Application Version	0x0001
Bootloader Start Address	0x0
Bootloader End Address	0x10A8

For more information on the bootloader and startup please refer to:

- Startup and Linking chapter in the [System Reference Guide](#)

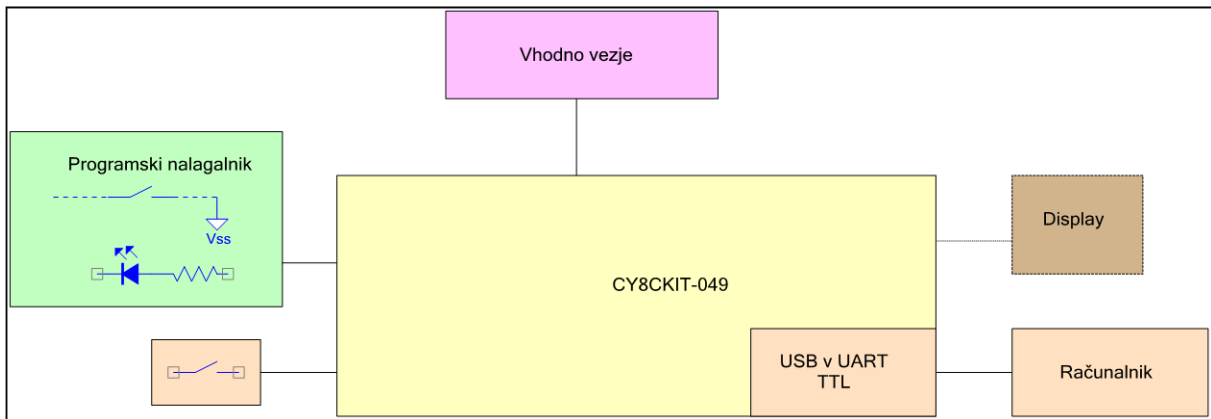
- Datasheet for [Bootloader and Bootloadable component](#)

8 Design Contents

This design's schematic content consists of the following 6 schematic sheets:

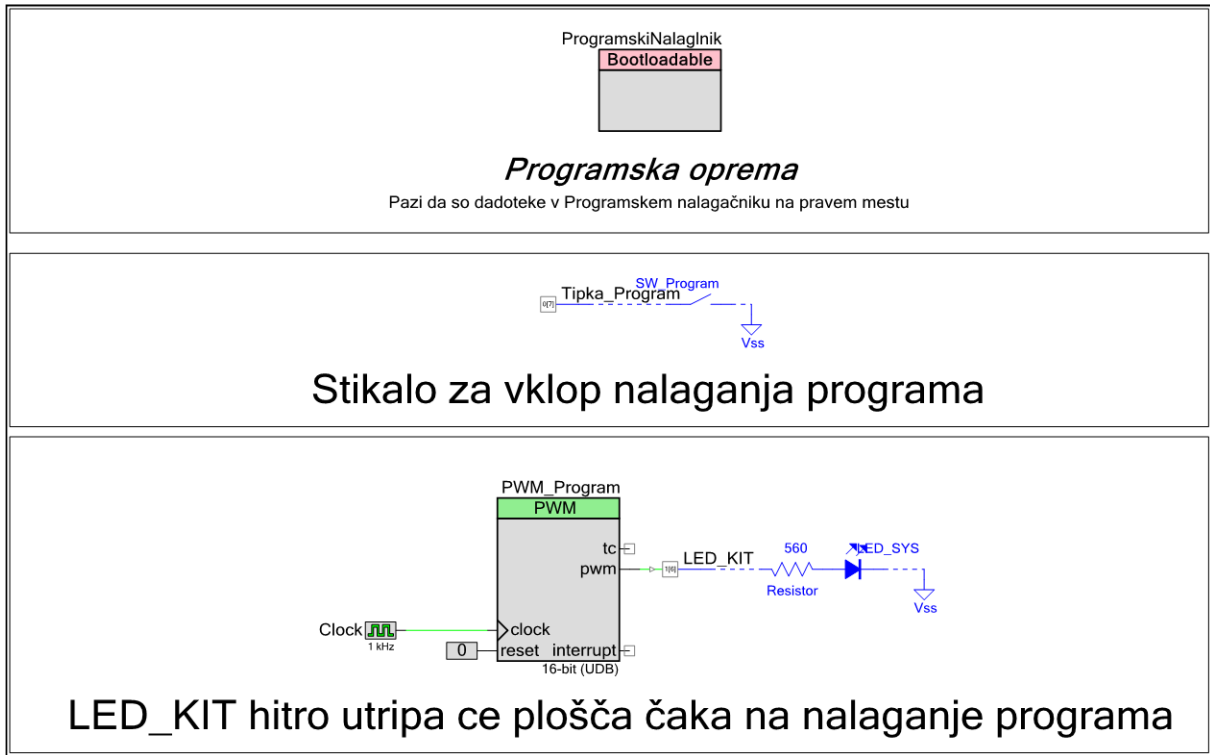
8.1 Schematic Sheet: BlokShema

Figure 6. Schematic Sheet: BlokShema



8.2 Schematic Sheet: Osnovno

Figure 7. Schematic Sheet: Osnovno

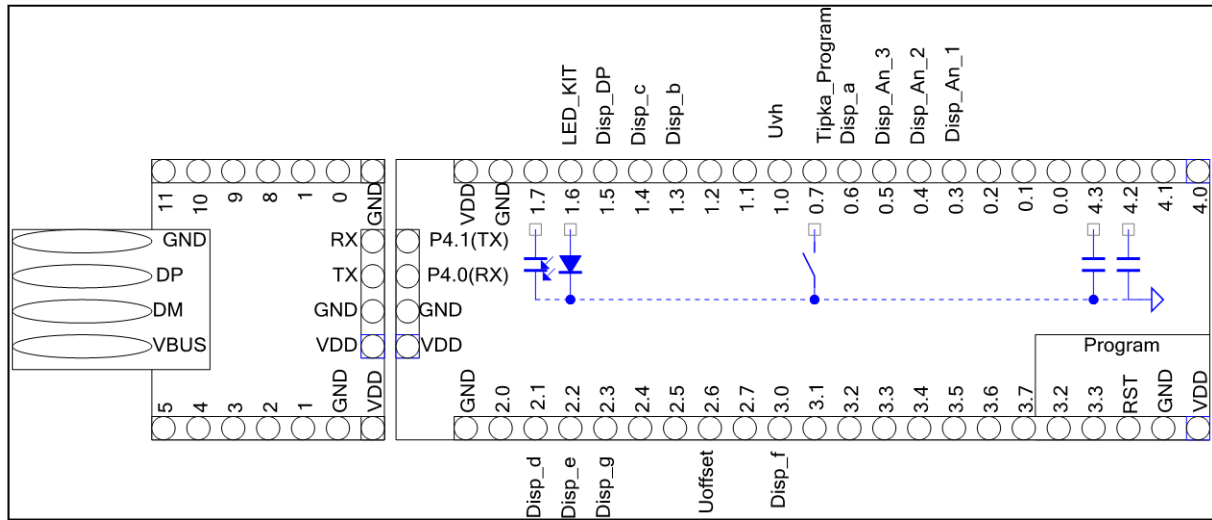


This schematic sheet contains the following component instances:

- Instance [ProgramskiNalaglnik](#) (type: Bootloadable_v1_50)
- Instance [PWM_Program](#) (type: PWM_v3_30)

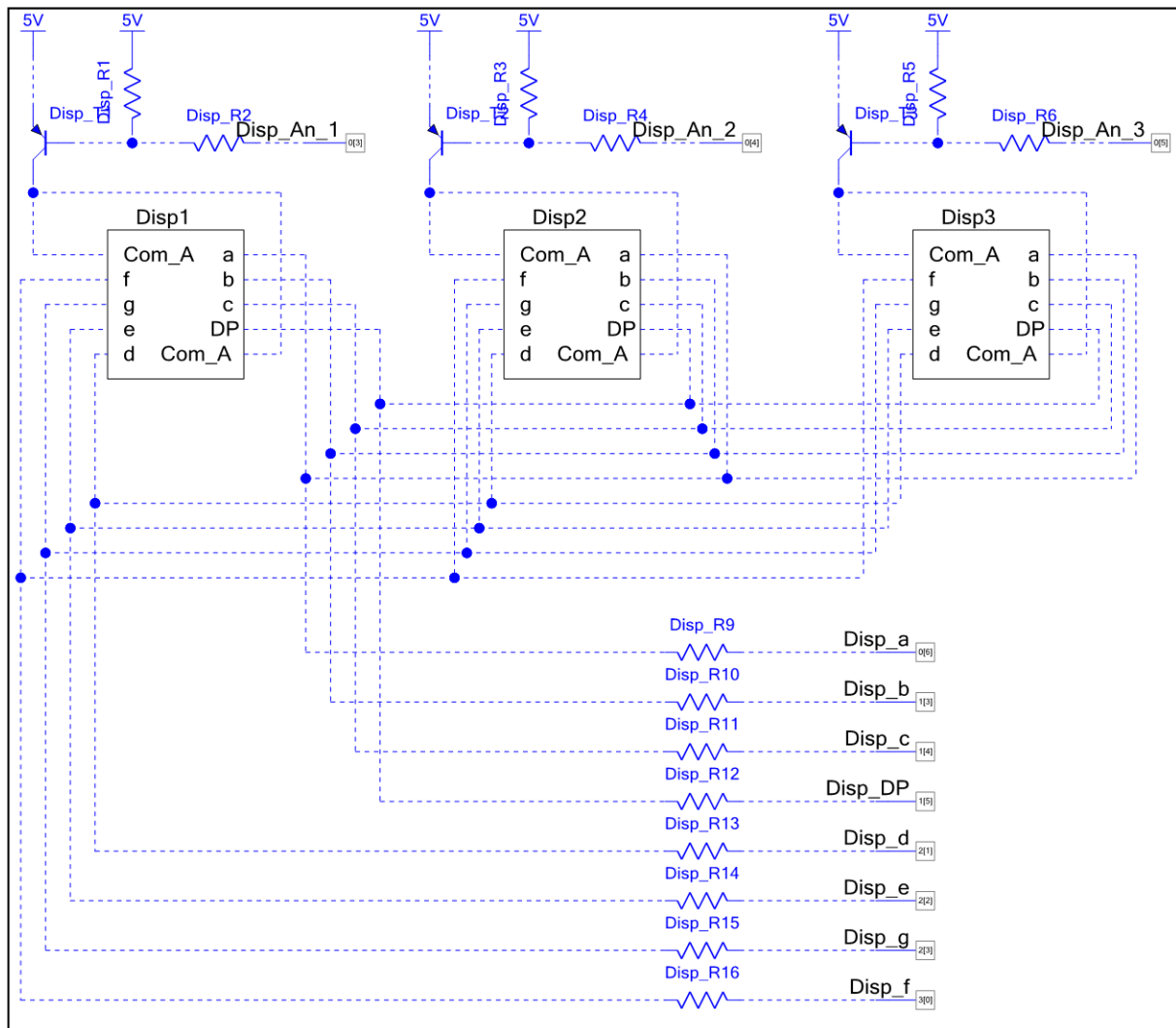
8.3 Schematic Sheet: CY8Ckit049

Figure 8. Schematic Sheet: CY8Ckit049



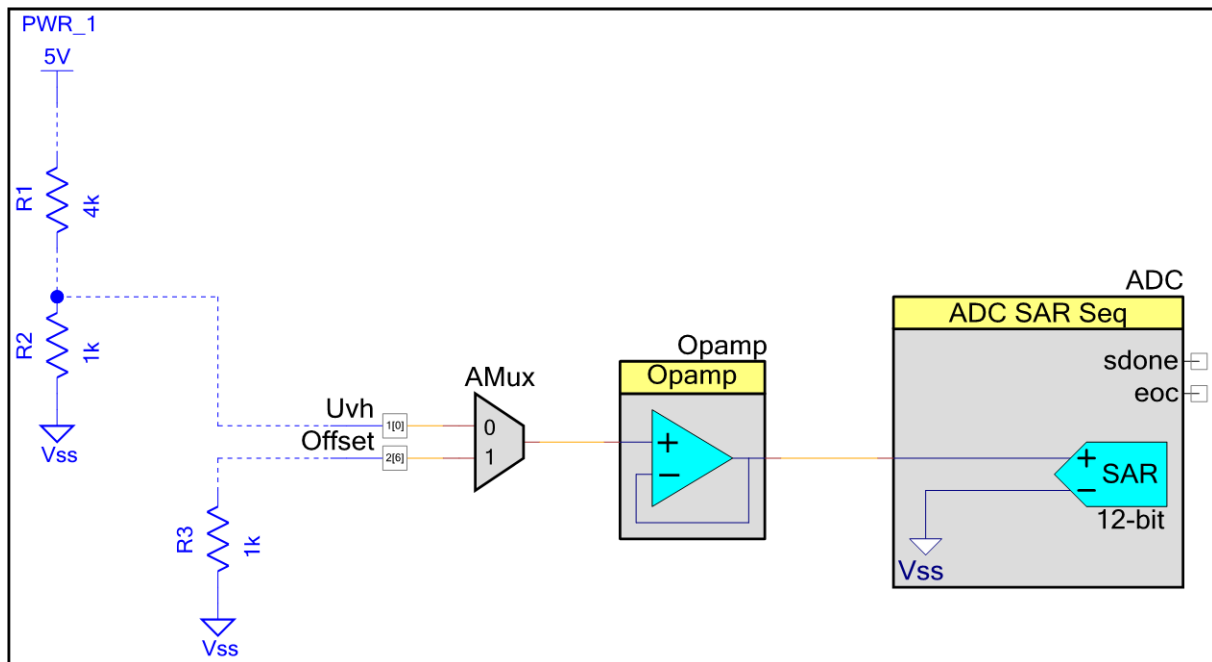
8.4 Schematic Sheet: Disp_LEDx3

Figure 9. Schematic Sheet: Disp_LEDx3



8.5 Schematic Sheet: Analog

Figure 10. Schematic Sheet: Analog

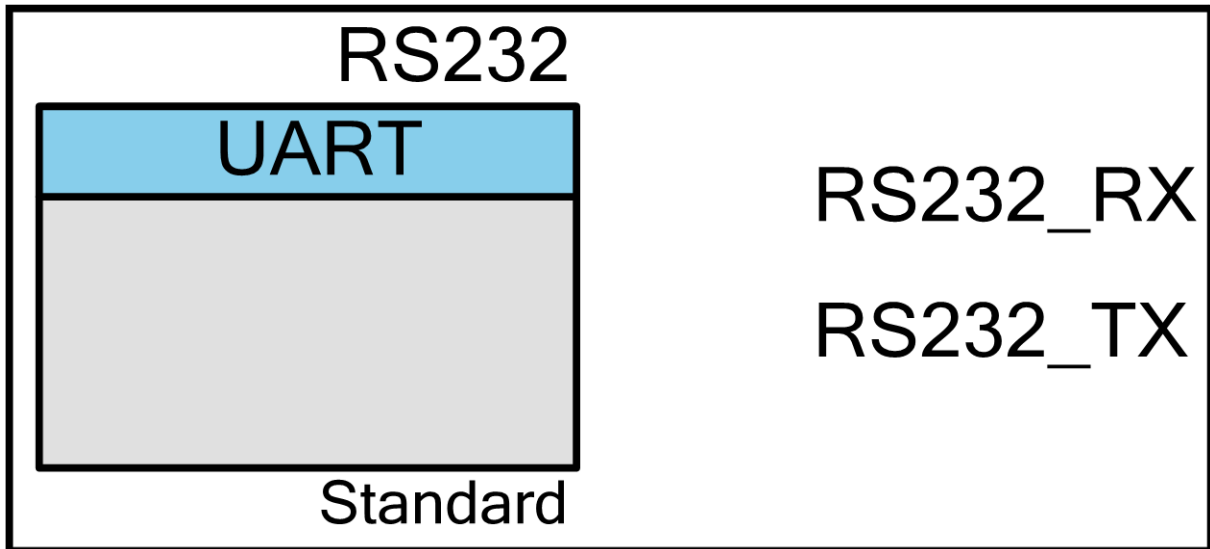


This schematic sheet contains the following component instances:

- Instance [ADC](#) (type: ADC_SAR_SEQ_P4_v2_50)
- Instance [AMux](#) (type: AMux_v1_80)
- Instance [Opamp](#) (type: OpAmp_P4_v1_20)

8.6 Schematic Sheet: Povezava

Figure 11. Schematic Sheet: Povezava



This schematic sheet contains the following component instances:

- Instance [RS232](#) (type: SCB_P4_v4_0)

9 Components

9.1 Component type: ADC_SAR_SEQ_P4 [v2.50]

9.1.1 Instance ADC

Description: PSoC 4 Sequencing Successive Approximation ADC

Instance type: ADC_SAR_SEQ_P4 [v2.50]

Datasheet: [online component datasheet for ADC_SAR_SEQ_P4](#)

Table 15. Component Parameters for ADC

Parameter Name	Value	Description
AdcAClock	4	Acquisition time in clock cycles for configuration A.
AdcAdjust	ScanRate	Timing parameter adjustable by the user.
AdcAlternateResolution	8	This parameter sets the alternate ADC resolution to either 8 or 10 bits.
AdcAvgMode	Fixed Resolution	This parameter sets how the averaging mode operates.
AdcAvgSamplesNum	2	This parameter sets the averaging rate for any channel that has its averaging option enabled.
AdcBClock	4	Acquisition time in clock cycles for configuration B.
AdcCClock	4	Acquisition time in clock cycles for configuration C.
AdcChannelsEnConf	1	This bitmask is intended to enable the channels for scanning during runtime.
AdcChannelsModeConf	0	Mode configuration for the channels (0 - Single, 1 - Differential)
AdcClock	Internal	Clock source type.
AdcClockFrequency	2999988	Specifies the internal clock frequency in Hz.
AdcCompareMode	Result < Low_Limit	This parameter sets the condition in which the limit condition will occur.
AdcDataFormatJustification	Right	This parameter sets whether the output data is left or right justified for a 16-bit word. For signed values, the result will be sign extended when configured in right justification mode.
AdcDClock	4	Acquisition time in clock cycles for configuration D.
AdcDifferentialResultFormat	Signed	This parameter sets the whether the result from a differential measurement is Signed or Unsigned.
AdcHighLimit	2047	This parameter sets the high limit for a limit compare.

Parameter Name	Value	Description
AdcInjChannelEnabled	false	Determines whether the symbol will display the injection channel.
AdcInputBufGain	Disable	Sets the input buffer gain or disables it.
AdcLowLimit	0	This parameter sets the low limit for a limit compare.
AdcMaxResolution	12	Sets the maximum resolution of the ADC in bits.
AdcSampleMode	FreeRunning	Sampling mode.
AdcSarMuxChannelConfig	0	Channels mode configuration for the multiplexer (0 - Single, 1 - Differential)
AdcSequencedChannels	1	Number of input signals that will be scanned. This excludes the injection channel.
AdcSingleEndedNegativeInput	Vss	Negative input source for single ended operation.
AdcSingleResultFormat	Signed	This parameter sets whether the result from a single ended measurement is Signed or Unsigned.
AdcSymbolHasSingleEndedInputChannel	false	Determines whether the configuration contains an external negative input.
AdcVrefSelect	Internal 1.024 volts, bypassed	The reference voltage that is used for the SAR ADC.
AdcVrefVoltage_mV	1024	The reference voltage value.
rm_int	false	Removes the internal interrupt
User Comments		Instance-specific comments.

9.2 Component type: AMux [v1.80]

9.2.1 Instance AMux

Description: Multiplexer used to route analog signals.

Instance type: AMux [v1.80]

Datasheet: [online component datasheet for AMux](#)

Table 16. Component Parameters for AMux

Parameter Name	Value	Description
AtMostOneActive	false	Limit to at most one active channel.
Channels	2	Channel count.
Isolation	Medium	Specify minimum, medium, or maximum switch control; affects channel isolation and switching time.
MuxType	Single	Select between single or differential inputs.
User Comments		Instance-specific comments.

9.3 Component type: Bootloadable [v1.50]

9.3.1 Instance ProgramskiNalaglnik

Description: Provides bootloadable application functionality.

Instance type: Bootloadable [v1.50]

Datasheet: [online component datasheet for Bootloadable](#)

Table 17. Component Parameters for ProgramskiNalaglnik

Parameter Name	Value	Description
appCustomID	0	Provides a 4 byte custom ID number to represent anything in the Bootloadable application.
appID	0	Provides a 2 byte number to represent the ID of the bootloadable application.
appVersion	1	Provides a 2 byte number to represent the version of the bootloadable application.
autoPlacement	true	Provides a method for PSoC Creator to place a Bootloadable application image at a specified location. If true, the image will be placed automatically. If false, the image will be placed at an address specified by the Placement Address option.
checksumExcludeSize	0	Provides a size in bytes of checksum exclude section
elfFilePath	..\..\..\Programs-kiNalagalniki\ProgramskiNalagalnik_CY8C42_001_6junij2017\UART_ProgramskiNalagalnik_42_001.elf	Provides a reference to the Bootloader application (.elf) that is associated with this Bootloadable application.
hexFilePath	..\..\..\Programs-kiNalagalniki\ProgramskiNalagalnik_CY8C42_001_6junij2017\UART_ProgramskiNalagalnik_42_001.hex	Provides a reference to the Bootloader application (.hex) that is associated with this Bootloadable application.
placementAddress	0	Allows specifying an address where the bootloadable application will be placed in the memory. Available only if the Automatic Application Image Placement option is true.
User Comments		Instance-specific comments.

9.4 Component type: OpAmp_P4 [v1.20]

9.4.1 Instance Opamp

Description: Opamp

Instance type: OpAmp_P4 [v1.20]

Datasheet: [online component datasheet for OpAmp_P4](#)

Table 18. Component Parameters for Opamp

Parameter Name	Value	Description
Compensation	High	Compensation is used to prevent unwanted oscillations in the output

Parameter Name	Value	Description
DeepSleepSupport	false	The component available in Deep Sleep
Mode	Follower	The mode of operation
OutputCurrent	Internal only	Selects the output mode
Power	Medium Power	The component power setting
User Comments		Instance-specific comments.

9.5 Component type: PWM [v3.30]

9.5.1 Instance PWM_Program

Description: 8 or 16-bit Pulse Width Modulator

Instance type: PWM [v3.30]

Datasheet: [online component datasheet for PWM](#)

Table 19. Component Parameters for PWM_Program

Parameter Name	Value	Description
CaptureMode	None	Defines the functionality of the capture Input. The parameter determines which signal on the capture input is required to capture the current count value to the FIFO.
CompareStatusEdgeSense	true	Enables edge sense detection on compare outputs for use in edge sensitive interrupts
CompareType1	Less	Sets the compare value comparison type setting for the compare 1 output
CompareType2	Less	Sets the compare value comparison type setting for the compare 2 output
CompareValue1	750	Compares Output 1 to value
CompareValue2	63	Compares Output 2 to value
DeadBand	Disabled	Defines whether dead band outputs are desired or not.
DeadTime	1	Defines the number of required dead band clock cycles
DitherOffset	0.00	Allows the user to implement dither to get more bits out of a 8 or 16 bit PWM.
EnableMode	Software Only	Specifies the method of enabling the PWM. This can be either hardware or software.
FixedFunction	false	Determines whether the fixed function counter timer is used or the UDB implementation is used.
InterruptOnCMP1	false	Enables the interrupt on compare1 true event
InterruptOnCMP2	false	Enables the interrupt on compare2 true event
InterruptOnKill	false	Enables the interrupt on a kill event
InterruptOnTC	false	Enables the interrupt on terminal count event

Parameter Name	Value	Description
KillMode	Disabled	Parameter to select the kill mode for build time.
MinimumKillTime	1	Sets the minimum number of clock cycles that a kill must be active on the outputs when KillMode is set to Minimum Kill Time mode
Period	1500	Defines the PWM period value
PWMMode	One Output	Defines the overall mode of the PWM
Resolution	16	Defines the bit width of the PWM (8 or 16 bits)
RunMode	Continuous	Defines the run mode options to be either continuous or one shot
TriggerMode	None	Determines the mode of starting the PWM, i.e. triggering the PWM counter to start
UseInterrupt	true	Enables the placement and usage of the status register
User Comments		Instance-specific comments.

9.6 Component type: SCB_P4 [v4.0]

9.6.1 Instance RS232

Description: Serial Communication Block (SCB)

Instance type: SCB_P4 [v4.0]

Datasheet: [online component datasheet for SCB_P4](#)

Table 20. Component Parameters for RS232

Parameter Name	Value	Description
EzI2cByteModeEnable	false	When the SCB mode is EZI2C, this parameter specifies the number of bits per FIFO data element. The byte mode – false: a 16-bit FIFO data element. The FIFO depth is 8 entries. The byte mode – true: an 8-bit FIFO data element. The FIFO depth is 16 entries. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
EzI2cClockFromTerm	false	When the SCB mode is EZI2C, this parameter provides a clock terminal to connect a clock outside the component.
EzI2cClockStretching	true	When the SCB mode is EZI2C, this parameter specifies whether the SCL is stretched while in EZI2C operation.

Parameter Name	Value	Description
EzI2cDataRate	100	When the SCB mode is EZI2C, this parameter defines EZI2C Data rate in kbps. The standard data rates are: 100, 400 and 1000 kbps.
EzI2cNumberOfAddresses	1	When the SCB mode is EZI2C, this parameter defines the number of I2C slave addresses that device respond to.
EzI2cPrimarySlaveAddress	8	When the SCB mode is EZI2C, this parameter specifies EZI2C primary 7-bits slave address (MSB ignored).
EzI2cSecondarySlaveAddress	9	When the SCB mode is EZI2C, this parameter specifies EZI2C secondary 7-bits slave address (MSB ignored). Only applicable when EZI2C clock stretching option is set.
EzI2cSubAddressSize	8	When the SCB mode is EZI2C, this parameter specifies the maximum size of the slave buffer that is exposed to the master: 8bits – maximum buffer size is 256 bytes, 16 bits – maximum buffer size is 65535 bytes.
EzI2cWakeEnable	false	When the SCB mode is EZI2C, this parameter enables wakeup from Deep Sleep on I2C address match event.
I2C Bus Voltage	3.3	When the SCB mode is I2C, this parameter specifies the voltage applied to the pull-up resistors on the I2C bus. Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2C Bus Voltage	3.3	When the SCB mode is EZI2C, this parameter specifies the voltage applied to the pull-up resistors on the I2C bus. Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2cAcceptAddress	false	When the SCB mode is I2C, this parameter specifies whether to accept the match slave address in RX FIFO or not. All slave matched addresses are ACKed. The user has to register the callback function to handle accepted addresses. This feature has to be used when more than one address support is required.

Parameter Name	Value	Description
I2cAcceptGeneralCall	false	When the SCB mode is I2C, this parameter specifies whether to accept the general call address. The general call address is ACKed when accepted and NAKed otherwise. The user has to register the callback function to handle the general call address.
I2cByteModeEnable	false	When the SCB mode is I2C, this parameter specifies the number of bits per FIFO data element. The byte mode – false: a 16-bit FIFO data element. The FIFO depth is 8 entries. The byte mode – true: an 8-bit FIFO data element. The FIFO depth is 16 entries. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
I2cClockFromTerm	false	When the SCB mode is I2C, this parameter provides a clock terminal to connect a clock outside the component.
I2cDataRate	100	When the SCB mode is I2C, this parameter specifies the data rate in kbps. The standard data rates are: 100, 400 and 1000 kbps.
I2cExternIntrHandler	false	When the SCB mode is I2C, this parameter specifies whether the I2C interrupt handler is configured in SCB_I2CInit(). This parameter is intended to be used by the PM/SM bus component. The modification parameter default value causes I2C mode failures.
I2cManualOversampleControl	true	When the SCB mode is I2C, this parameter specifies the method of calculating the oversampling as manual or automatic.
I2cMode	Slave	When the SCB mode is I2C, this parameter defines the I2C operation mode as: Slave, Master, Multi-Master or Multi-Master-Slave.
I2cOvsFactor	16	When the SCB mode is I2C, this parameter defines the oversampling factor of SCBCLK.
I2cOvsFactorHigh	8	When the SCB mode is I2C, this parameter defines the high oversampling factor of SCBCLK. Only applicable for I2C Master modes.

Parameter Name	Value	Description
I2cOvsFactorLow	8	When the SCB mode is I2C, this parameter defines the low oversampling factor of SCBCLK. Only applicable for I2C Master modes.
I2cSlaveAddress	8	When the SCB mode is I2C, this parameter specifies the I2C 7-bits slave address (MSB ignored).
I2cSlaveAddressMask	254	When the SCB mode is I2C, this parameter specifies the I2C Slave address mask. Bit value 0 – excludes bit from address comparison. Bit value 1 – the bit needs to match with the corresponding bit of the I2C slave address.
I2cWakeEnable	false	When the SCB mode is I2C, this parameter enables wakeup from Deep Sleep on an I2C address match event.
ScbMisoSdaTxEnable	true	This parameter defines the availability of the spi_miso_i2c_sda_uart_tx pin.
ScbMode	UART	This parameter defines the mode of operation for the SCB component.
ScbMosiSclRxEnable	true	This parameter defines the availability of the spi_mosi_i2c_scl_uart_rx pin.
ScbRxWakeIrqEnable	false	This parameter defines the availability of the spi_mosi_i2c_scl_uart_rx_wake pin.
ScbSclkEnable	false	This parameter defines the availability of the sclk pin.
ScbSs0Enable	false	This parameter defines the availability of the ss0 pin.
ScbSs1Enable	false	This parameter defines the availability of the ss1 pin.
ScbSs2Enable	false	This parameter defines the availability of the ss2 pin.
ScbSs3Enable	false	This parameter defines the availability of the ss3 pin.
Show EZI2C Terminals	false	When the SCB mode is EZI2C, this parameter removes internal pins and expose signals to terminals. The exposed terminals must be connected to the pins.
Show I2C Terminals	false	When the SCB mode is I2C, this parameter removes internal pins and expose signals to terminals. The exposed terminals must be connected to the pins.

Parameter Name	Value	Description
Show SPI Terminals	false	When the SCB mode is SPI, this parameter removes internal pins and expose signals to terminals. The exposed terminals must be connected to the pins or SmartIO component.
Show UART Terminals	false	When the SCB mode is UART, this parameter removes internal pins and expose signals to terminals. The exposed terminals must be connected to the pins or SmartIO component.
Slew Rate	Fast	When the SCB mode is EZI2C, this parameter specifies the slew rate settings of the I2C pins. For devices supporting GPIO Over-Voltage Tolerance (GPIO_OVT) pins, I2C FM+ options should be used when I2C data rate is greater than 400 kbps. This option also requires the I2C bus voltage to be defined. Refer to the Device Datasheet to determine which pins are GPIO_OVT capable.
Slew Rate	Fast	When the SCB mode is I2C, this parameter specifies the slew rate settings of the I2C pins. For devices supporting GPIO Over-Voltage Tolerance (GPIO_OVT) pins, I2C FM+ options should be used when I2C data rate is greater than 400 kbps. This option also requires the I2C bus voltage to be defined. Refer to the Device Datasheet to determine which pins are GPIO_OVT capable.
SpiBitRate	1000	When the SCB mode is SPI, this parameter specifies the Bit rate in kbps (up to 8000 kbps); the actual rate may differ based on available clock frequency and component settings. This parameter has no effect if the Clock from terminal parameter is enabled.
SpiBitsOrder	MSB First	When the SCB mode is SPI, this parameter defines the bit order as: MSB first or LSB first.

Parameter Name	Value	Description
SpiByteModeEnable	false	<p>When the SCB mode is SPI, this parameter specifies the number of bits per FIFO data element.</p> <p>The byte mode – false: a 16-bit FIFO data element. The FIFO depth is 8 entries.</p> <p>The byte mode – true: an 8-bit FIFO data element. The FIFO depth is 16 entries.</p> <p>Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.</p>
SpiClockFromTerm	false	<p>When the SCB mode is SPI, this parameter provides a clock terminal to connect a clock outside the component.</p>
SpiFreeRunningSclk	false	<p>When the SCB mode is SPI, this parameter specifies the SCLK generation by the master as: gated or free running (continuous).</p> <p>Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.</p>
SpiInterruptMode	None	<p>When the SCB mode is SPI, this parameter specifies the interrupt mode. None: Removes all interrupt support. Internal: Leaves the interrupt SCBIRQ inside the component - the interrupt terminal becomes invisible. External: Provides an interrupt terminal to connect an interrupt outside the component.</p>
SpiIntrMasterSpiDone	false	<p>When the SCB mode is SPI, this parameter enables the SCB.INTR_M. SPI_DONE interrupt source.</p> <p>SCB.INTR_M. SPI_DONE: all data are sent into TX FIFO and the TX FIFO and the shifter register are emptied.</p> <p>Only applicable for SPI Master mode.</p>
SpiIntrRxFull	false	<p>When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.FULL interrupt source.</p> <p>SCB.INTR_RX.FULL trigger condition: RX FIFO is full.</p>

Parameter Name	Value	Description
SpilntrRxNotEmpty	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.NOT_EMPTY interrupt source. SCB.INTR_RX.NOT_EMPTY trigger condition: RX FIFO is not empty. There is at least one entry to get data from.
SpilntrRxOverflow	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.OVERFLOW interrupt source. SCB.INTR_RX.OVERFLOW trigger condition: attempt to write to a full RX FIFO.
SpilntrRxTrigger	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.TRIGGER interrupt source. SCB.INTR_RX.TRIGGER trigger condition: remains active until RX FIFO has more entries than the value specified by SpiRxTriggerLevel.
SpilntrRxUnderflow	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_RX.UNDERFLOW interrupt source. SCB.INTR_RX.UNDERFLOW trigger condition: attempt to read from an empty RX FIFO.
SpilntrSlaveBusError	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_SLAVE.BUS_ERROR interrupt source. SCB.INTR_SLAVE.BUS_ERROR trigger condition: slave select line is deselected at an unexpected time in the SPI transfer. Only applicable for SPI Slave mode.
SpilntrTxEmpty	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_TX.EMPTY interrupt source. SCB.INTR_TX.EMPTY trigger condition: TX FIFO is empty.
SpilntrTxNotFull	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_TX.NOT_FULL interrupt source. SCB.INTR_TX.NOT_FULL trigger condition: TX FIFO is not full. There is at least one entry to put data.

Parameter Name	Value	Description
SpiIntrTxOverflow	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_TX.OVERFLOW interrupt source. SCB.INTR_TX.OVERFLOW trigger condition: attempt to write to a full TX FIFO.
SpiIntrTxTrigger	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_TX.TRIGGER interrupt source. SCB.INTR_TX.TRIGGER trigger condition: remains active until TX FIFO has fewer entries than the value specified by SpiTxTriggerLevel.
SpiIntrTxUnderflow	false	When the SCB mode is SPI, this parameter enables the SCB.INTR_TX.UNDERFLOW interrupt source. SCB.INTR_TX.UNDERFLOW trigger condition: attempt to read from an empty TX FIFO.
SpiLateMisoSampleEnable	false	When the SCB mode is SPI, this parameter enables late sampling of the MISO line by the master.
SpiMedianFilterEnable	false	When the SCB mode is SPI, this parameter applies a digital 3 tap median filter to the SPI input line.
SpiMode	Slave	When the SCB mode is SPI, this parameter selects SPI mode of operation as: Slave or Master.
SpiNumberOfRxDataBits	8	When the SCB mode is SPI, this parameter specifies the number of data bits inside the SPI byte/word for RX direction.
SpiNumberOfSelectLines	1	When the SCB mode is SPI, this parameter defines the number of slave select lines. The SPI Slave has only one slave select line. The SPI Master has up to 4 lines.
SpiNumberOfTxDataBits	8	When the SCB mode is SPI, this parameter define the number of data bits inside the SPI byte/word for TX direction.
SpiOvsFactor	16	When the SCB mode is SPI, this parameter defines the oversampling factor of SCBCLK.
SpiRemoveMiso	false	When the SCB mode is SPI, this parameter removes the MISO pin.
SpiRemoveMosi	false	When the SCB mode is SPI, this parameter removes the MOSI pin.

Parameter Name	Value	Description
SpiRemoveSclk	false	When the SCB mode is SPI, this parameter removes the SCLK pin.
SpiRxBufferSize	8	When the SCB mode is SPI, this parameter defines the size of the RX buffer.
SpiRxOutputEnable	false	When the SCB mode is SPI, this parameter enables the RX trigger output terminal of the component. This terminal must be connected to the DMA input trigger or left unconnected. Only applicable for devices which have a DMA controller.
SpiRxTriggerLevel	7	When the SCB mode is SPI, this parameter defines the number of entries in the RX FIFO to control the SCB.INTR_ - RX.TRIGGER interrupt event or RX DMA trigger output.
SpiSclkMode	CPHA = 0, CPOL = 0	When the SCB mode is SPI, this parameter defines the serial clock phase (CPHA) and polarity (CPOL).
SpiSs0Polarity	Active Low	When the SCB mode is SPI, this parameter specifies active polarity of slave select 0. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
SpiSs1Polarity	Active Low	When the SCB mode is SPI, this parameter specifies active polarity of slave select 1. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
SpiSs2Polarity	Active Low	When the SCB mode is SPI, this parameter specifies active polarity of slave select 2. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
SpiSs3Polarity	Active Low	When the SCB mode is SPI, this parameter specifies active polarity of slave select 3. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
SpiSubMode	Motorola	When the SCB mode is SPI, this parameter defines the sub mode of the SPI as: Motorola, TI(Start Coincides), TI(Start Precedes), or National Semiconductor.

Parameter Name	Value	Description
SpiTransferSeparation	Continuous	When the SCB mode is SPI, this parameter defines the type of SPI transfers separation as: continuous or separated.
SpiTxBufferSize	8	When the SCB mode is SPI, this parameter defines the size of the TX buffer.
SpiTxOutputEnable	false	When the SCB mode is SPI, this parameter enables the TX trigger output terminal of the component. This terminal must be connected to the DMA input trigger or left unconnected. Only applicable for devices which have a DMA controller.
SpiTxTriggerLevel	0	When the SCB mode is SPI, this parameter defines the number of entries in the TX FIFO to control the SCB.INTR_ - TX.TRIGGER interrupt event or TX DMA trigger output.
SpiWakeEnable	false	When the SCB mode is SPI, this parameter enables wakeup from Deep Sleep on slave select event.
UartByteModeEnable	false	<p>When the SCB mode is UART, this parameter specifies the number of bits per FIFO data element.</p> <p>The byte mode – false: a 16-bit FIFO data element. The FIFO depth is 8 entries.</p> <p>The byte mode – true: an 8-bit FIFO data element. The FIFO depth is 16 entries.</p> <p>Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.</p>
UartClockFromTerm	false	When the SCB mode is UART, this parameter provides a clock terminal to connect a clock outside the component.
UartCtsEnable	false	<p>When the SCB mode is UART, this parameter enables the cts input.</p> <p>Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.</p>
UartCtsPolarity	Active Low	<p>When the SCB mode is UART, this parameter specifies active polarity of an input cts signal.</p> <p>Only applicable for devices other than PSoC 4000/PSoC 4100/PSoC 4200.</p>

Parameter Name	Value	Description
UartDataRate	115200	When the SCB mode is UART, this parameter specifies the Baud rate in bps (up to 1000 kbps); the actual rate may differ based on available clock frequency and component settings. This parameter has no effect if the Clock from terminal parameter is enabled.
UartDirection	TX + RX	When the SCB mode is UART, this parameter enables RX or TX direction or both simultaneously.
UartDropOnFrameErr	false	When the SCB mode is UART, this parameter defines whether the data is dropped from RX FIFO on a frame error event.
UartDropOnParityErr	false	When the SCB mode is UART, this parameter determines whether the data is dropped from RX FIFO on a parity error event.
UartInterruptMode	None	When the SCB mode is UART, this parameter specifies the interrupt mode. None: Removes all interrupt support. Internal: Leaves the interrupt SCBIRQ inside the component - the interrupt terminal becomes invisible. External: Provides an interrupt terminal to connect an interrupt outside component.
UartIntrRxBreakDetected	false	This parameter enables the RX break detection interrupt source to trigger the interrupt output.
UartIntrRxFrameErr	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.FRAME_ERROR interrupt source. SCB.INTR_RX.FRAME_ERROR trigger condition: frame error in received data frame.
UartIntrRxFull	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.FULL interrupt source. SCB.INTR_RX.FULL trigger condition: RX FIFO is full.
UartIntrRxNotEmpty	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.NOT_EMPTY interrupt source. SCB.INTR_RX.NOT_EMPTY trigger condition: RX FIFO is not empty. There is at least one entry to get data from.

Parameter Name	Value	Description
UartIntrRxOverflow	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.OVERFLOW interrupt source. SCB.INTR_RX.OVERFLOW trigger condition: attempt to write to a full RX FIFO.
UartIntrRxParityErr	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.PARITY_ERROR interrupt source. SCB.INTR_RX.PARITY_ERROR trigger condition: parity error in received data frame.
UartIntrRxTrigger	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.TRIGGER interrupt source. SCB.INTR_RX.TRIGGER trigger condition: remains active until RX FIFO has more entries than the value specified by UartRxTriggerLevel.
UartIntrRxUnderflow	false	When the SCB mode is UART, this parameter enables the SCB.INTR_RX.UNDERFLOW interrupt source. SCB.INTR_RX.UNDERFLOW trigger condition: attempt to read from an empty RX FIFO.
UartIntrTxEmpty	false	When the SCB mode is UART, this parameter enables the SCB.INTR_TX.EMPTY interrupt source. SCB.INTR_TX.EMPTY trigger condition: TX FIFO is empty.
UartIntrTxNotFull	false	When the SCB mode is UART, this parameter enables the SCB.INTR_TX.NOT_FULL interrupt source. SCB.INTR_TX.NOT_FULL trigger condition: TX FIFO is not full. There is at least one entry to put data.
UartIntrTxOverflow	false	When the SCB mode is UART, this parameter enables the SCB.INTR_TX.OVERFLOW interrupt source. SCB.INTR_TX.OVERFLOW trigger condition: attempt to write to a full TX FIFO.

Parameter Name	Value	Description
UartIntrTxTrigger	false	When the SCB mode is UART, this parameter enables the SCB.INTR_TX.TRIGGER interrupt source. SCB.INTR_TX.TRIGGER trigger condition: remains active until TX FIFO has fewer entries than the value specified by UartTxTriggerLevel.
UartIntrTxUartDone	false	When the SCB mode is UART, this parameter enables the SCB.INTR_TX.UART_DONE interrupt source. SCB.INTR_TX.UART_DONE trigger condition: all data are sent in to TX FIFO and the transmit FIFO and the shifter register are emptied.
UartIntrTxUartLostArb	false	When the SCB mode is UART, this parameter enables the SCB.INTR_TX.UART_ARB_LOST interrupt source. SCB.INTR_TX.UART_ARB_LOST trigger condition: UART lost arbitration, the value driven on the TX line is not the same as the value observed on the RX line. This event is useful when the transmitter and the receiver share a TX/RX line. Only applicable for UART SmartCard mode.
UartIntrTxUartNack	false	When the SCB mode is UART, this parameter enables the SCB.INTR_TX.UART_NACK interrupt source. SCB.INTR_TX.UART_NACK trigger condition: UART transmitter received a negative acknowledgement. Only applicable for UART SmartCard mode.
UartIntrTxUnderflow	false	When the SCB mode is UART, this parameter enables the SCB.INTR_TX.UNDERFLOW interrupt source. SCB.INTR_TX.UNDERFLOW trigger condition: attempt to read from an empty TX FIFO.
UartIrdaLowPower	false	When the SCB mode is UART, this parameter enables the low power receiver option. Only applicable for UART IrDA mode.
UartIrdaPolarity	Non-Inverting	When the SCB mode is UART, this parameter inverts the incoming RX line signal. Only applicable for UART IrDA mode.

Parameter Name	Value	Description
UartMedianFilterEnable	false	When the SCB mode is UART, this parameter applies a digital 3 tap median filter to the UART input line.
UartMpEnable	false	When the SCB mode is UART, this parameter enables the UART multi-processor mode. Only applicable for UART Standard mode.
UartMpRxAcceptAddress	false	When the SCB mode is UART, this parameter define whether to put the matched UART address into RX FIFO. Only applicable for UART multi-processor mode.
UartMpRxAddress	2	When the SCB mode is UART, this parameter defines the UART address. Only applicable for UART multi-processor mode.
UartMpRxAddressMask	255	When the SCB mode is UART, this parameter defines the address mask in multi-processor operation mode. Bit value 0 – excludes bit from address comparison. Bit value 1 – the bit needs to match with the corresponding bit of the UART address. Only applicable for UART multi-processor mode.
UartNumberOfDataBits	8 bits	When the SCB mode is UART, this parameter defines the number of data bits inside the UART byte/word.
UartNumberOfStopBits	1 bit	When the SCB mode is UART, this parameter defines the number of Stop bits.
UartOvsFactor	8	When the SCB mode is UART, this parameter defines the oversampling factor of SCBCLK.
UartParityType	None	When the SCB mode is UART, this parameter applies UART parity check as Odd or Even or discards the parity entirely.
UartRtsEnable	false	When the SCB mode is UART, this parameter enables the rts output. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.

Parameter Name	Value	Description
UartRtsPolarity	Active Low	When the SCB mode is UART, this parameter specifies active polarity of the output rts signal. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartRtsTriggerLevel	4	When the SCB mode is UART, this parameter specifies the number of entries in the RX FIFO to activate the rts output signal. When the receiver FIFO has fewer entries than the UartRtsTriggerLevel, an rts output signal is activated. Applicable only for devices other than PSoC 4000/PSoC 4100/PSoC 4200.
UartRxBreakWidth	11	This parameter specifies the break width in bits.
UartRxBufferSize	8	When the SCB mode is UART, this parameter defines the size of the RX buffer.
UartRxOutputEnable	false	When the SCB mode is UART, this parameter enables the RX trigger output terminal of the component. This terminal must be connected to the DMA input trigger or left unconnected. Only applicable for devices which have a DMA controller.
UartRxTriggerLevel	7	When the SCB mode is UART, this parameter defines the number of entries in the RX FIFO to trigger control the SCB.INTR_RX.TRIGGER interrupt event or RX DMA trigger output.
UartSmCardRetryOnNack	false	When the SCB mode is UART, this parameter defines whether to send a message again when a NACK response is received. Only applicable for UART SmartCard mode.
UartSubMode	Standard	When the SCB mode is UART, this parameter defines the sub mode of UART as: Standard, SmartCard or IrDA.
UartTxBufferSize	8	When the SCB mode is UART, this parameter defines the size of the TX buffer.

Parameter Name	Value	Description
UartTxOutputEnable	false	When the SCB mode is UART, this parameter enables the TX trigger output terminal of the component. This terminal must be connected to the DMA input trigger or left unconnected. Only applicable for devices which have a DMA controller.
UartTxTriggerLevel	0	When the SCB mode is UART, this parameter defines the number of entries in the TX FIFO to control the SCB.INTR_TX.TRIGGER interrupt event or TX DMA trigger output.
UartWakeEnable	false	When the SCB mode is UART, this parameter enables the wakeup from Deep Sleep on start bit event. The actual wakeup source is RX GPIO. The skip start UART feature allows it to continue receiving bytes.
User Comments		Instance-specific comments.

10 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the [System Reference Guide](#)
 - Software base types
 - Hardware register types
 - Compiler defines
 - Cypress API return codes
 - Interrupt types and macros
- Registers
 - The full PSoC 4 register map is covered in the [PSoC 4 Registers Technical Reference Manual](#)
 - Register Access chapter in the [System Reference Guide](#)
 - § CY_GET API routines
 - § CY_SET API routines
- System Functions chapter in the [System Reference Guide](#)
 - General API routines
 - CyDelay API routines
 - CyVd Voltage Detect API routines
- Power Management
 - Power Supply and Monitoring chapter in the [PSoC 4 Technical Reference Manual](#)
 - Low Power Modes chapter in the [PSoC 4 Technical Reference Manual](#)
 - Power Management chapter in the [System Reference Guide](#)
 - § CyPm API routines
- Watchdog Timer chapter in the [System Reference Guide](#)
 - CyWdt API routines